MLT ISO SPI Board

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T he isolated SPI module is designed for applications, where SPI signals need to be transferred over longer distances than usually. It is based on Linear's LTC6820. The board is designed as two layer stack-up, with GND plane on the bottom layer and signal traces and components at the top layer. Signals and power are supplied over standard 100mil (2.54mm) pitch IDC header.
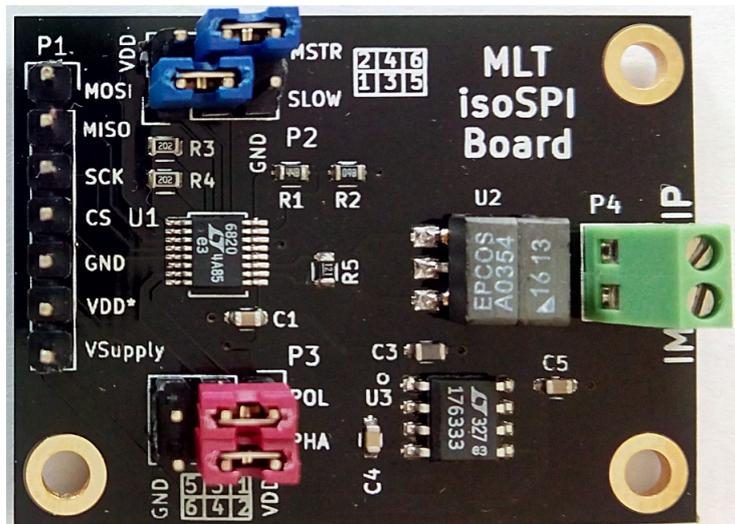

Figure 1: *photo of the board*

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The License is attatched at the end of this document as well as a Guide to the CERN OHL v.1.2.

Please feel free to give your highly appreciated feedback, comments and suggestions. Or ask any questions about the board. We'll be glad to answer or help you.

Specification

- Dimension: 40.005 mm x 30.099 mm (1.575" x 1.185")

- 1 Mbps Isolated SPI Data Communication at 10m

- 500 kbps Isolated SPI Data Communication at 100m

- Galvanic Isolation Barrier using standard transformer (1500V)

- Requires no software changes in most SPI systems

- 3.5V to 15V power supply

- SPI mode can be adjust via on-board jumpers

- can act as Master or Slave (adjustable via jumper)

- screw terminal for twisted pair cable (i.e. as in CAT5 Ethernet cable)

For more details and description , please read the data sheet of the LTC 6820. Below is an possible application scenario of the module.
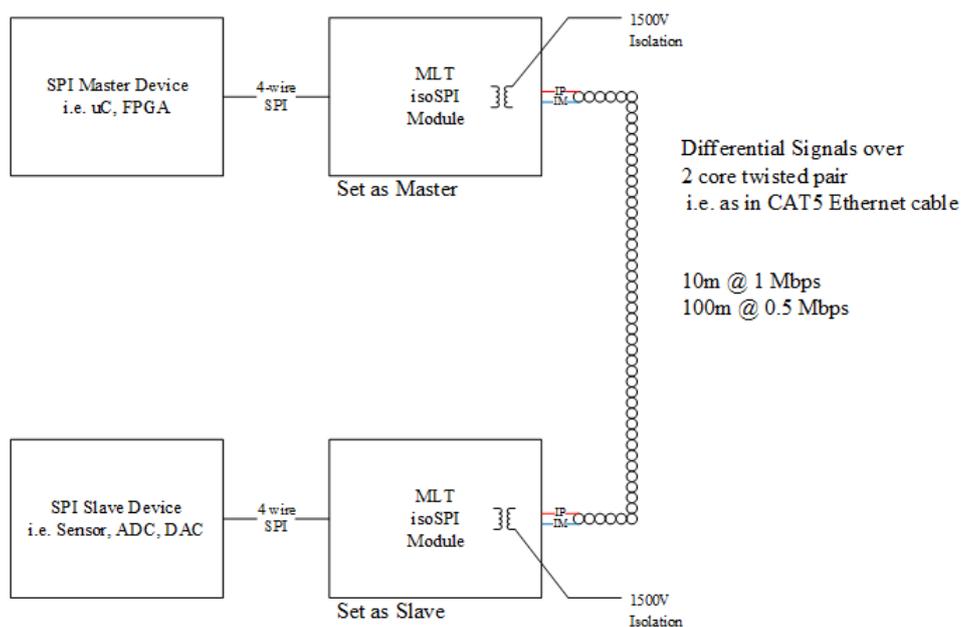
Figure 2: *Application*

Jumper Settings & Pin header

Pin Header P1

P1 is the pin header for the SPI signals and power supply. It has an standard pitch of 100 mils (2.45 mm).

Table 1: *Pin Header P1*

PIN	SIGNAL	FUNCTION
1	MOSI	SPI Signals
1	MISO	SPI Signals
1	SCK	SPI Signals
1	CS	SPI Signals
1	GND	
1	VDD	Digital Supply Voltage (Output U3)
1	VS	Supply Voltage (Input U3)

You can supply about 3.5V to 15V to the board. The on-board LDO LTC1763 will generate 3.3V for supply the LTC 6820. For more details, see the specification for the LTC 1763.

In case you need different voltage levels for the SPI signals, you can supply 2.7V to 5.5V to the board via VDD pin(P1[6]). In this case you should remove U3 (LTC1763). It is also possible to use any other pin compatible power supply with 8-SOIC footprint or ones from the same family. See the data sheet for the LTC1763 for more details.

It is also possible to use the board with two different SPI signal levels(level shifting).

Jumper P2, Master & clock speed

With P2 you adjust the clock frequency and the Master/Slave mode.

Figure 3: *Jumper Settings Master, Slow*

SLOW pin

For clock speeds below 200 kHz, the jumper must be in position 1-3(VDD). For clock frequencies 200-1000 kHz, the jumper must be in position 3-5(GND).

Table 2: *Jumper P2, SLOW pin*

| POSITION	VOLTAGE LEVEL	CLOCK FREQUENCY
1-3	VDD	<200 kHz
3-5	GND	200-1000 kHz

MSTR pin

For using this board as SPI Master, the jumper must be in position 2-4 (VDD). For using this board as SPI Slave, the jumper must be in position 4-6 (GND). The default position is 4-6 (Slave).

Table 3: *Jumper P2, MSTR pin*

POSITION	VOLTAGE LEVEL	FUNCTION
2-4	VDD	Master
4-6	GND	Slave

Jumper P3, SPI MODE

With P3 you adjust the SPI mode. Phase and Polarity.
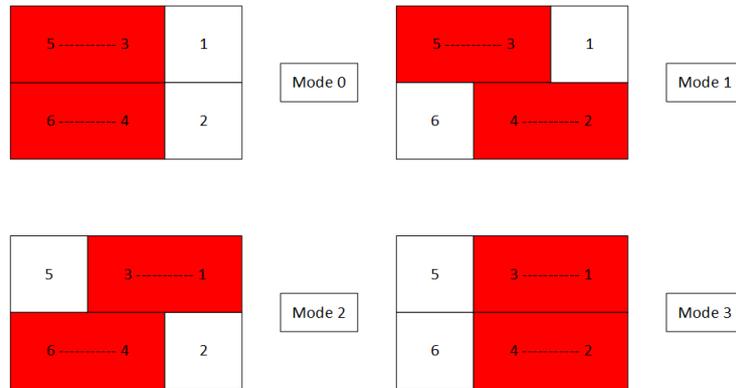
Figure 4: *Jumper Settings SPI Mode*

Table 4: *Jumper P3, SPI mode*

MODE	POL	PHA	POSITION	DESCRIPTION
0	0	0	5-3, 6-4	SCK Idles Low, Latches on Rising Edge
1	0	1	5-3, 4-2	SCK Idles Low, Latches on Falling Edge
2	1	0	3-1, 6-4	SCK Idles High, Latches on Rising Edge
3	1	1	3-1, 4-2	SCK Idles High, Latches on Falling Edge

Screw Terminal P4

The screw terminal P4 is the connector for the twisted pair cable. The differential signal pulses are transferred or received over this connector on IP and IM.
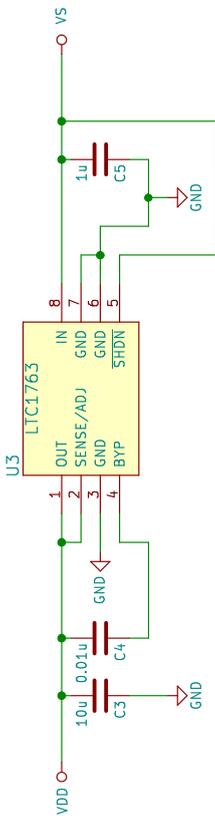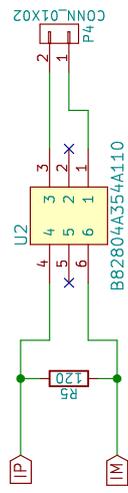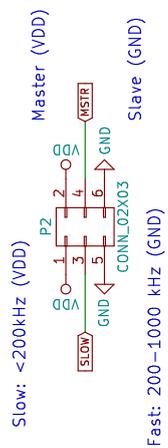
Connect IP with IP and IM with IM respectively.

Bias Resistors R1, R2

The bias resistors are selected for a good compromise between power consumption and noise immunity. Ib is set to 0.5mA, which is good for most application and allow for 50m cable length with a normal CAT5 twisted pair. If you need/want to change these resistors, read the data sheet the section "Application Information" for more details how to calculate these resistors.

Attachments

1. Board Schematics

2. CERN OHL v1.2

3. CERN OHL v1.2 How-to-Guide
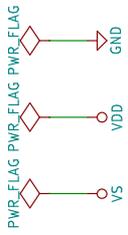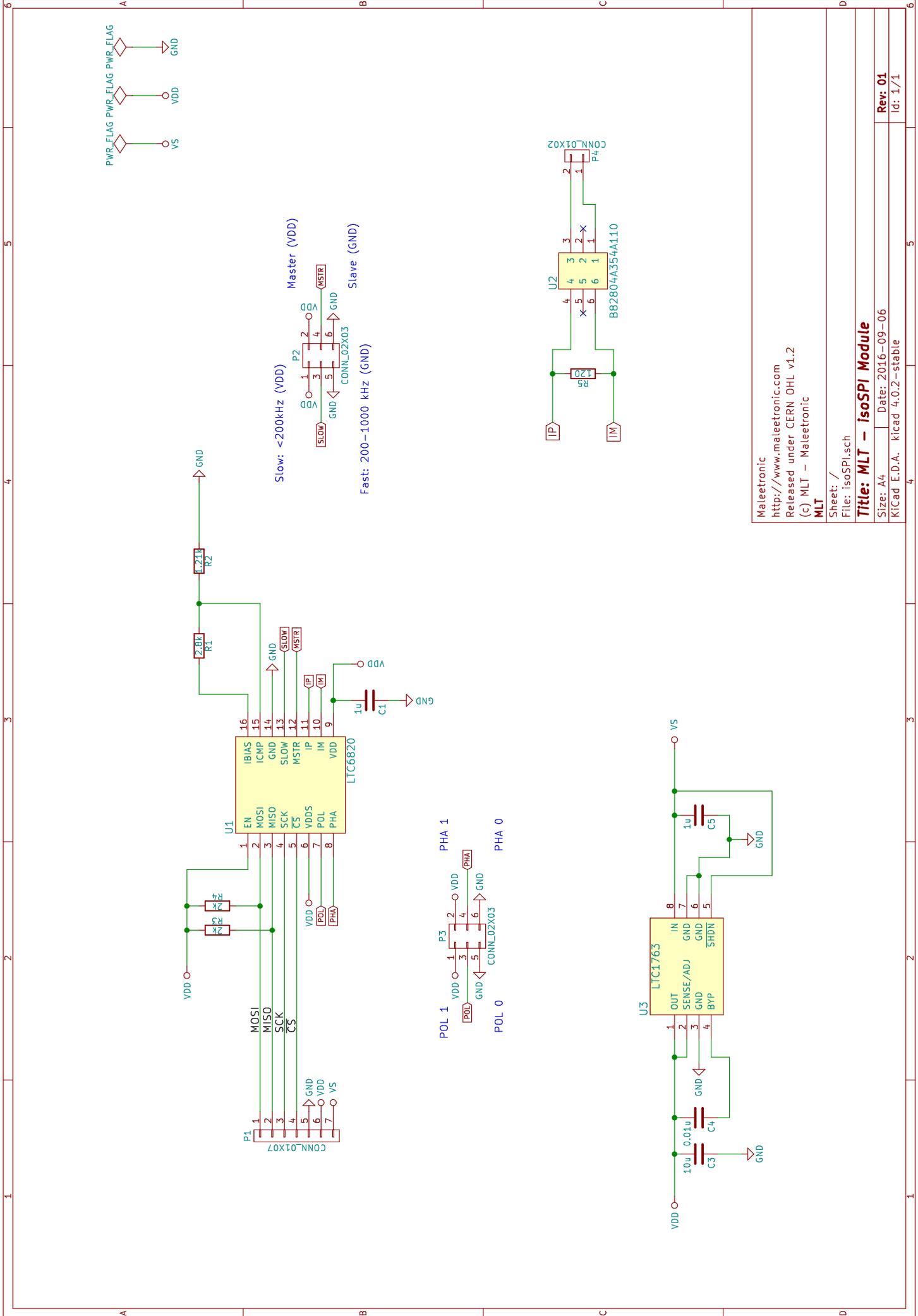
PWR_FLAG PWR_FLAG PWR_FLAG

GND
VDD
VS

Master (VDD)
Slave (GND)

Slow: <200kHz (VDD)

Fast: 200–1000 kHz (GND)

P2
CONN_02X03
MSTR
SLOW
VDD
VDD
GND
GND

P4
CONN_01X02
U2
B82804A354A110
R5 120
IP
IM

GND
R2 1.21k
R1 2.8k

U1
LTC6820
IBIAS ICMP GND SLOW MSTR IP IM VDD
EN MOSI MISO SCK CS VDDS POL PHA

SLOW
MSTR
IP
IM
VDD
C1 1u
GND

R4 2k
R3 2k
VDD

VDD
POL
PHA

MOSI
MISO
SCK
CS

P1
CONN_01X07
GND
VDD
VS

P3
CONN_02X03
PHA
VDD
POL
GND

PHA 1
PHA 0
POL 1
POL 0

U3
LTC1763
IN GND GND SHDN
OUT SENSE/ADJ GND BYP

VS
C5 1u
GND

GND
C3 10u
C4 0.01u
GND
VDD

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