



PIC18F1230/1330

18/20-Pin Enhanced Flash Microcontrollers with Power Control PWM, nanoWatt Technology and A/D

High-Performance RISC CPU:

- C compiler optimized architecture/instruction set
- Up to 10 MIPS operation
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 31-level, software accessible hardware stack
- 8 x 8 Single-Cycle Hardware Multiplier

14-Bit Power Control PWM Module:

- Up to 3 channels with complementary outputs
- Edge or center-aligned operation
- Flexible dead-band generator
- Hardware Fault protection input
- Simultaneous update of duty cycle and period
- Flexible special event trigger output
- Outputs are safely driven during debugging

Flexible Oscillator Structure:

- Four Crystal modes up to 40 MHz
- Two External modes up to 40 MHz
- 4x PLL can be used to drive Internal Oscillator or External Crystal modes
- Internal Oscillator block:
 - User-selectable frequencies: 31 kHz to 32 MHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown of device if clock fails

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Two-Speed Oscillator Start-up

Analog Features:

- 10-bit, up to 4-channel Analog-to-Digital Converter module (A/D):
 - Auto-acquisition time
 - Up to 100 ksps conversion rate
 - Conversion available during Sleep
- Three Analog Comparators
- On-board voltage reference
- External voltage reference input
- Programmable 16-level Low-Voltage Detection (LVD) module:
 - Interrupt on Low-Voltage Detection
- Programmable Brown-out Reset (BOR)

Peripheral Highlights:

- High-current sink/source 25 mA/25 mA
- Four external interrupts/interrupt-on-change pins
- Enhanced USART module:
 - Supports RS-485, RS-232, LIN 1.2
 - Auto-wake-up on Start bit
 - Auto-Baud Detect

Special Microcontroller Features:

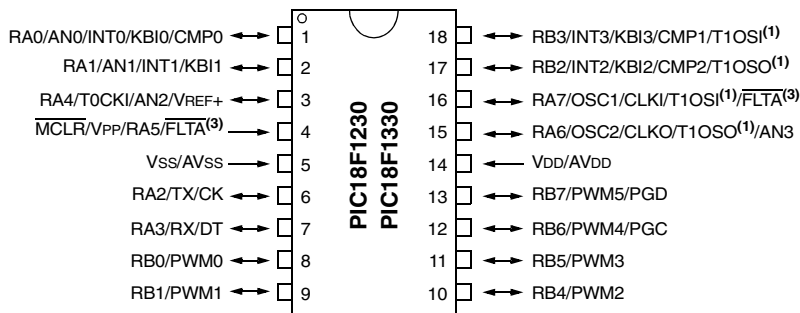
- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Flash/Data EEPROM Retention > 100 years
- Self-programmable under software control
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
 - 2% accuracy over VDD and Temperature
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- Enhanced In-Circuit Debug (ICD) via two pins

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	Comparators	14-Bit PWM (ch)	EUSART	Timers (16-Bit)
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)						
PIC18F1230	4096	2048	256	128	16	4	3	6	Y	2
PIC18F1330	8192	4096	256	128	16	4	3	6	Y	2

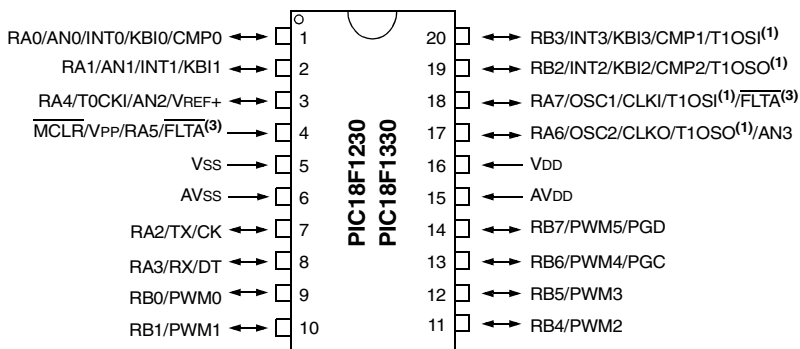
PIC18F1230/1330

Pin Diagrams*

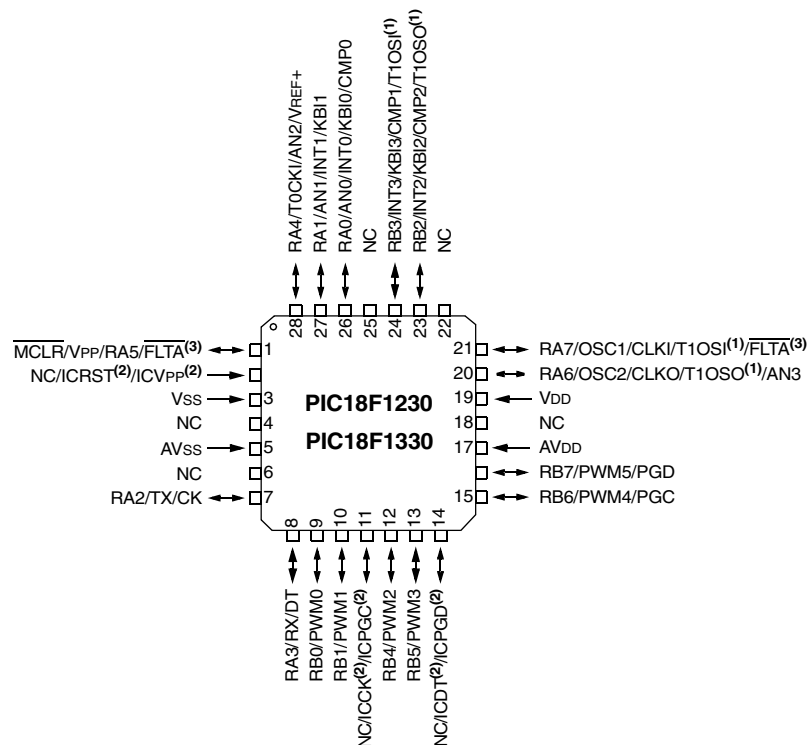
18-Pin PDIP, SOIC



20-Pin SSOP



28-Pin QFN



* Pinouts are subject to change.

Note 1: Placement of T1OSI and T1OSO depends on the configuration of the oscillator.

Note 2: Pin feature is dependent on device configuration.

Note 3: Placement of FLTA depends on the value of the corresponding configuration bit.

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