NCV1124

Dual Variable-Reluctance Sensor Interface IC

The NCV1124 is a monolithic integrated circuit designed primarily to condition signals from sensors used to monitor rotating parts.

The NCV1124 is a dual channel device. Each of the two identical channels interfaces with a variable−reluctance sensor, and continuously compares the sensor output signal to a user−programmable internal reference. An alternating input signal of appropriate amplitude at IN1 or IN2 will result in a rectangular waveform at the corresponding OUT terminal, suitable for interface to either standard microprocessors or standard logic families.

A diagnostic input, common to both channels, provides a means to test for degradation or loss of the physical connector to both sensors.

Typical Applications

- Anti−Skid Braking and Traction Control
- Vehicle Stability Control
- Drive Belt Slippage Detection
- Crankshaft/Camshaft Position Sensing

Features

- Two Independent Channels
- Internal Hysteresis
- Built−In Diagnostic Mode
- Designed to Work from a 5.0 V ±10% Supply
- Site and Control for Automotive Applications
- Pb−Free Packages are Available

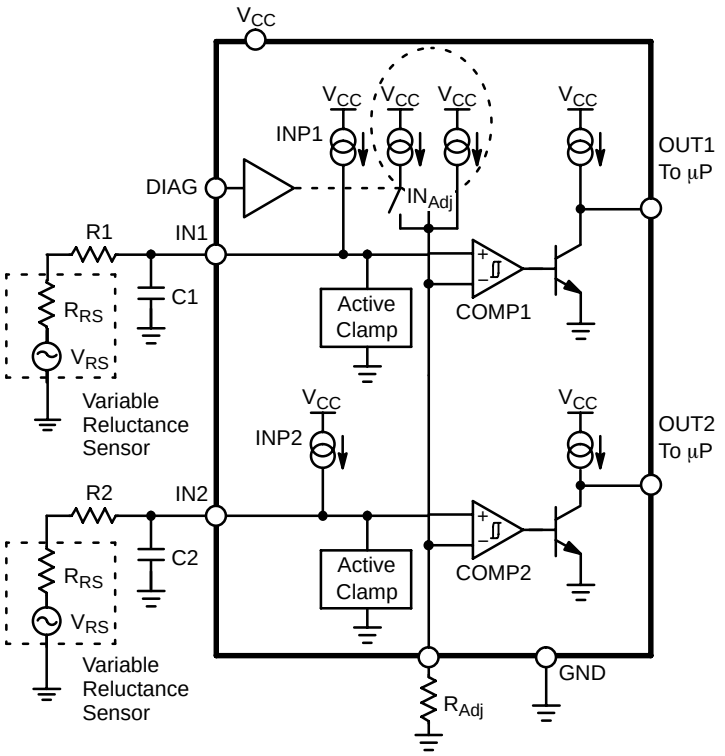

Figure 1. Block Diagram

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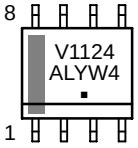
http://onsemi.com

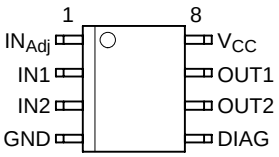
SO−8
CASE 751

MARKING DIAGRAM



V1124	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MAXIMUM RATINGS

Rating	Value	Unit
Storage Temperature Range	−65 to 150	°C
Ambient Operating Temperature	−40 to 125	°C
Supply Voltage Range (continuous)	−0.3 to 7.0	V
Input Voltage Range (at any input, R1 = R2 = 22 k)	−250 to 250	V
Maximum Junction Temperature	150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	240 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.

ELECTRICAL CHARACTERISTICS ($4.5\ V < V_{CC} < 5.5\ V$, $-40°C < T_A < 125°C$, $V_{DIAG} = 0$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{CC} SUPPLY					
Operating Current Supply	V_{CC} = 5.0 V	−	−	5.0	mA
Sensor Inputs					
Input Threshold − Positive	V_{DIAG} = Low V_{DIAG} = High	135 135	160 160	185 185	mV mV
Input Threshold − Negative	V_{DIAG} = Low V_{DIAG} = High	−185 135	−160 160	−135 185	mV mV
Input Bias Current (INP1, INP2)	V_{IN} = 0.336 V	−16	−11	−6.0	μA
Input Bias Current (DIAG)	V_{DIAG} = 0 V	−	−	1.0	μA
Input Bias Current Factor (K_I) ($IN_{Adj} = INP \times K_I$)	V_{IN} = 0.336 V, V_{DIAG} = Low V_{IN} = 0.336 V, V_{DIAG} = High	− 152	100 155	− 157	%INP %INP
Bias Current Matching	INP1 or INP2 to IN_{Adj}, V_{IN} = 0.336 V	−1.0	0	1.0	μA
Input Clamp − Negative	I_{IN} = −50 μA I_{IN} = −12 mA	−0.5 −0.5	−0.25 −0.30	0 0	V V
Input Clamp − Positive	I_{IN} = +12 mA	5.0	7.0	9.8	V
Output Low Voltage	I_{OUT} = 1.6 mA	−	0.2	0.4	V
Output High Voltage	I_{OUT} = −1.6 mA	V_{CC} − 0.5	V_{CC} − 0.2	−	V
Mode Change Time Delay	−	0	−	20	μs
Input to Output Delay	I_{OUT} = 1.0 mA	−	1.0	20	μs
Output Rise Time	C_{LOAD} = 30 pF	−	0.5	2.0	μs
Output Fall Time	C_{LOAD} = 30 pF	−	0.05	2.0	μs
Open−Sensor Positive Threshold	V_{DIAG} = High, $R_{IN(Adj)}$ = 40 k. Note 2	29.4	54	86.9	kΩ
Logic Inputs					
DIAG Input Low Threshold	−	−	−	$0.2 \times V_{CC}$	V
DIAG Input High Threshold	−	$0.7 \times V_{CC}$	−	−	V
DIAG Input Resistance	$V_{IN} = 0.3 \times V_{CC}$, V_{CC} = 5.0 V $V_{IN} = V_{CC}$, V_{CC} = 5.0 V	8.0 8.0	22 22	70 70	kΩ kΩ

2. This parameter is guaranteed by design, but not parametrically tested in production.

PACKAGE PIN DESCRIPTION

PIN # SO−8	PIN SYMBOL	FUNCTION
1	IN_{Adj}	External resistor to ground that sets the trip levels of both channels. Functions for both diagnostic and normal mode
2	IN1	Input to channel 1
3	IN2	Input to channel 2
4	GND	Ground
5	DIAG	Diagnostic mode switch. Normal mode is low
6	OUT2	Output of channel 2
7	OUT1	Output of channel 1
8	V_{CC}	Positive 5.0 volt supply input

ORDERING INFORMATION

Device	Package	Shipping†
NCV1124DG	SO−8 NB (Pb−Free)	98 Units / Rail
NCV1124DR2G	SO−8 NB (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

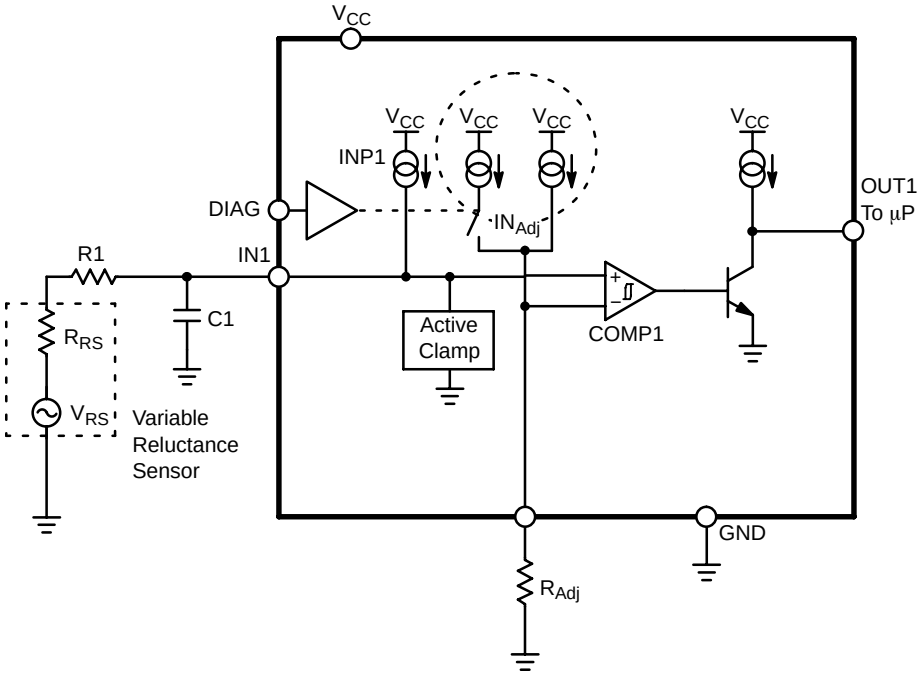


Figure 2. Application Diagram

THEORY OF OPERATION

NORMAL OPERATION

Figure 2 shows one channel of the NCV1124 along with the necessary external components. Both channels share the IN_{Adj} pin as the negative input to a comparator. A brief description of the components is as follows:

V_{RS} − Ideal sinusoidal, ground referenced, sensor output − amplitude usually increases with frequency, depending on loading.

R_{RS} − Source impedance of sensor.

R1/R_{Adj} − External resistors for current limiting and biasing.

INP1/IN_{Adj} − Internal current sources that determine trip points via $R1/R_{Adj}$.

COMP1 − Internal comparator with built−in hysteresis set at 160 mV.

OUT1 − Output 0 V − 5.0 V square wave with the same frequency as V_{RS}.

By inspection, the voltage at the (+) and (−) terminals of COMP1 with V_{RS} = 0V are:

$$V^+ = INP1(R1 + R_{RS}) \quad (1)$$

$$V^- = IN_{Adj} \times R_{Adj} \quad (2)$$

As V_{RS} begins to rise and fall, it will be superimposed on the DC biased voltage at V^+.

$$V^+ = INP1(R1 + R_{RS}) + V_{RS} \quad (3)$$

To get comparator COMP1 to trip, the following condition is needed when crossing in the positive direction,

$$V^+ > V^- + V_{HYS} \quad (4)$$

(V_{HYS} is the built−in hysteresis set to 160 mV), or when crossing in the negative direction,

$$V^+ < V^- - V_{HYS} \quad (5)$$

Combining equations 2, 3, and 4, we get:

$$INP1(R1 + R_{RS}) + V_{RS} > IN_{Adj} \times R_{Adj} + V_{HYS} \quad (6)$$

therefore,

$$V_{RS(+TRP)} < IN_{Adj} \times R_{Adj} - INP1(R1 + R_{RS}) + V_{HYS} \quad (7)$$

It should be evident that tripping on the negative side is:

$$V_{RS(-TRP)} < IN_{Adj} \times R_{Adj} - INP1(R1 + R_{RS}) - V_{HYS} \quad (8)$$

In normal mode,

$$INP1 = IN_{Adj} \quad (9)$$

We can now re−write equation (7) as:

$$V_{RS(+TR)} > INP1(R_{Adj} - R1 - R_{RS}) + V_{HYS} \quad (10)$$

By making

$$R_{Adj} = R1 + R_{RS} \quad (11)$$

you can detect signals with as little amplitude as V_{HYS}.

A design example is given in the applications section.

OPEN SENSOR PROTECTION

The NCV1124 has a DIAG pin that when pulled high (5.0 V), will increase the IN_{Adj} current source by roughly 50%.

Equation (7) shows that a larger $V_{RS(+TRP)}$ voltage will be needed to trip comparator COMP1. However, if no V_{RS} signal is present, then we can use equations 1, 2, and 4 (equation 5 does not apply in this mode) to get:

$$INP1(R1 + R_{RS}) > INP1 \times K_I \times R_{Adj} + V_{HYS} \quad (12)$$

Since R_{RS} is the only unknown variable we can solve for R_{RS},

$$R_{RS} = \frac{INP1 \times K_I \times R_{Adj} + V_{HYS}}{INP1} - R1 \quad (13)$$

Equation (13) shows that if the output switches states when entering the diag mode with V_{RS} = 0, the sensor impedance must be greater than the above calculated value. This can be very useful in diagnosing intermittent sensor.

INPUT PROTECTION

As shown in Figure 2, an active clamp is provided on each input to limit the voltage on the input pin and prevent substrate current injection. The clamp is specified to handle ±12 mA. This puts an upper limit on the amplitude of the sensor output. For example, if R1 = 20 k, then

$$V_{RS(MAX)} = 20\ k \times 12\ mA = 240\ V$$

Therefore, the $V_{RS(pk-pk)}$ voltage can be as high as 480 V.

The NCV1124 will *typically* run at a frequency up to 1.8 MHz if the input signal does not activate the positive or negative input clamps. Frequency performance will be lower when the positive or negative clamps are active. *Typical* performance will be up to a frequency of 680 kHz with the clamps active.

CIRCUIT DESCRIPTION

Figure 3 shows the part operating near the minimum input thresholds. As the sin wave input threshold is increased, the low side clamps become active (Figure 4). Increasing the amplitude further (Figure 5), the high−side clamp becomes active. These internal clamps allow for voltages up to −250 V and 250 V on the sensor side of the setup (with R1 = R2 = 22 k) (reference the diagram page 1).

Figure 6 shows the effect using the diagnostic (DIAG) function has on the circuit. The input threshold (negative) is switched from a threshold of −160 mV to +160 mV when DIAG goes from a low to a high. There is no hysteresis when DIAG is high.

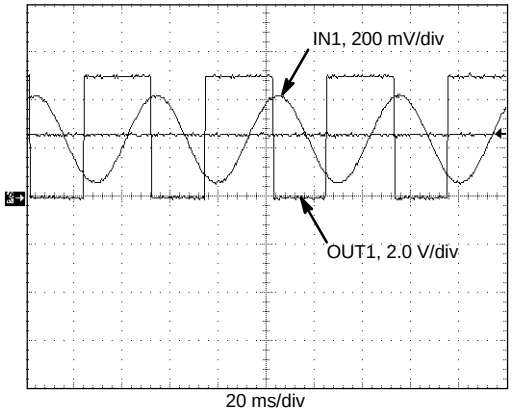


Figure 3. Minimum Threshold Operation

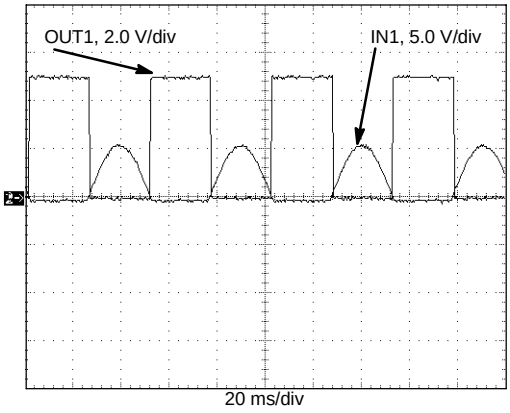


Figure 4. Low−Side Clamp

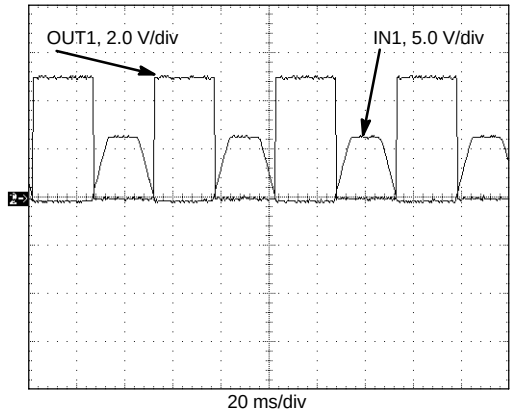


Figure 5. Low− and High−Side Clamps

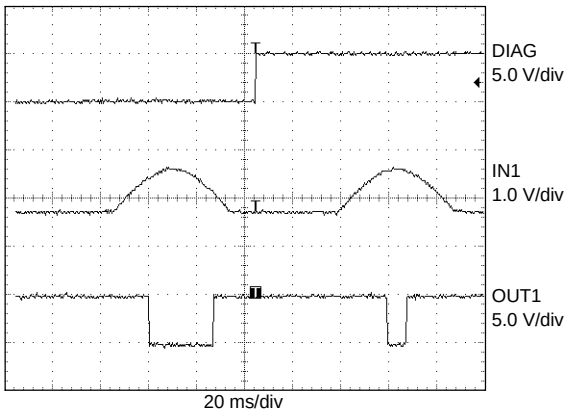


Figure 6. Diagnostic Operation

APPLICATION INFORMATION

Referring to Figure 2, the following will be a design example given these system requirements:

$$R_{RS} = 1.5\ k\Omega\ (> 12\ k\Omega \text{ is considered open})$$

$$V_{RS(MAX)} = 120\ V_{pk}$$

$$V_{RS(MIN)} = 250\ mV_{pk}$$

$$F_{VRS} = 10\ kHz\ @\ V_{RS(MIN)} = 40\ V_{pk-pk}$$

1. Determine tradeoff between R1 value and power rating. (use 1/2 watt package)

$$P_D = \frac{\left(\frac{120}{\sqrt{2}}\right)^2}{R1} < 1/2\ W$$

Set R1 = 15 k. (The clamp current will then be 120/15 k = 8.0 mA, which is less than the 12 mA limit.)

2. Determine R_{Adj}

Set R_{Adj} as close to R1 + R_{RS} as possible.

Therefore, R_{Adj} = 17 k.

3. Determine $V_{RS(+TRP)}$ using equation (7).

$$V_{RS(+TRP)} = 11\mu A \times 17\ k - 11\mu A(15\ k + 1.5\ k) + 160\ r$$

$$V_{RS(+TRP)} = 166\ mV \text{ typical}$$
(easily meets 250 mV minimum)

4. Calculate worst case $V_{RS(+TRP)}$

Examination of equation (7) and the spec reveals the worst case trip voltage will occur when:

V_{HYS} = 180 mV

IN_{Adj} = 16 μA

INP1 = 15 μA

R1 = 14.25 k (5% low)

R_{Adj} = 17.85 k (5% High)

$$V_{RS(+)MAX} = 16\ \mu A(17.85\ k) - 15\mu A(14.25\ k + 1.5\ k) + 180\ mV = 229\ mV$$

which is still less than the 250 mV minimum amplitude of the input.

5. Calculate C1 for low pass filtering

Since the sensor guarantees 40 V_{pk-pk} @ 10 kHz, a low pass filter using R1 and C1 can be used to eliminate high frequency noise without affecting system performance.

$$\text{Gain Reduction} = \frac{0.29\ V}{20\ V} = 0.0145 = -36.7\ dB$$

Therefore, a cut−off frequency, f_C, of 145 Hz could be used.

$$C1 \le \frac{1}{2\pi f_C R1} \le 0.07\ \mu F$$

Set C1 = 0.047 μF.

6. Calculate the minimum R_{RS} that will be indicated as an open circuit. (DIAG = 5.0 V)

Rearranging equation (7) gives

$$R_{RS} = \frac{\left[V_{HYS} + [INP1 \times K_I \times R_{Adj}] - V_{RS(+TRP)}\right]}{INP1} - R1$$

But, V_{RS} = 0 during this test, so it drops out.

Using the following as worst case Low and High:

	Worst Case Low (R_{RS})	Worst Case High (R_{RS})
IN_{Adj}	23.6 μA = 15 μA × 1.57	10.7 μA = 7.0 μA × 1.53
R_{Adj}	16.15 k	17.85 k
V_{HYS}	135 mV	185 mV
INP1	16 μA	6.0 μA
R1	15.75 k	14.25 k
K_I	1.57	1.53

$$R_{RS} = \frac{135\ mV + 23.6\ \mu A \times 16.15\ k}{16\ \mu A} - 15.75\ k = 16.5\ k$$

Therefore,

$$R_{RS(MIN)} = 16.5\ k \text{ (meets 12 k system spec)}$$

and,

$$R_{RS(MAX)} = \frac{185\ mV + 10.7\ \mu A \times 17.85\ k}{6.0\mu A} - 14.25\ k = 48.4\ k$$

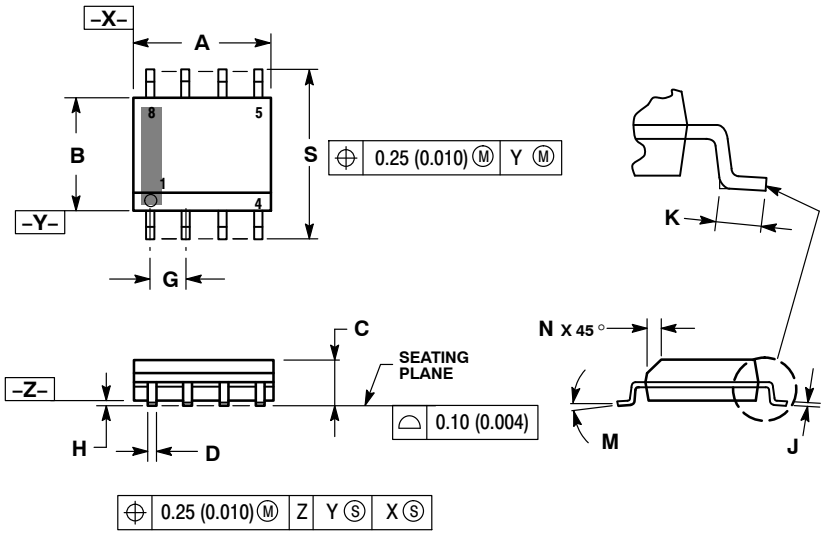
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

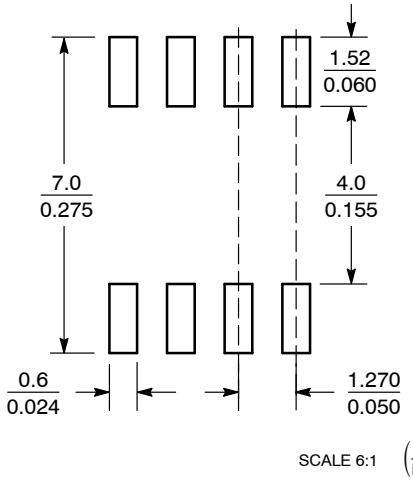
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

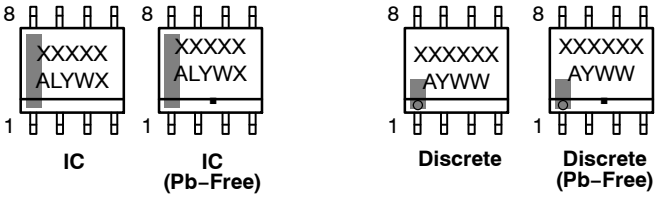
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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