

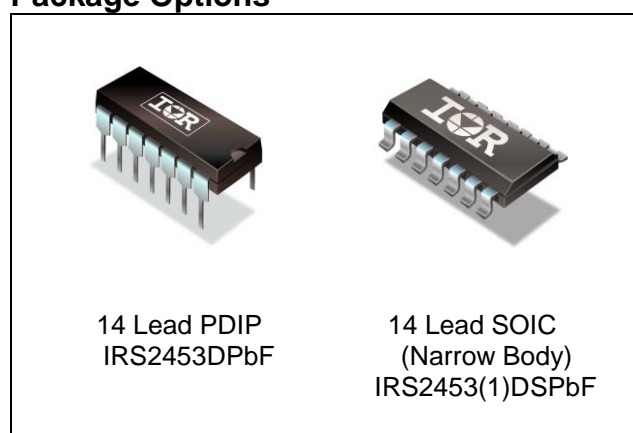
### Features

- Integrated 600 V full-bridge gate driver
- CT, RT programmable oscillator
- 15.6 V Zener clamp on  $V_{CC}$
- Micropower startup
- Logic level latched shutdown pin
- Non-latched shutdown on CT pin ( $1/6$ th  $V_{CC}$ )
- Internal bootstrap FETs
- Excellent latch immunity on all inputs & outputs
- ESD protection on all pins
- 14-lead SOIC or PDIP package
- 0.5 or 1.0 $\mu$ s (typ.) internal dead time
- RoHS compliant

### Product Summary

Topology	Full-bridge
$V_{OFFSET}$	600 V
$I_{O+}$ & $I_{O-}$ (typical)	180 mA & 260 mA
Deadtime (typical)	1.0 $\mu$ s (IRS2453D) 0.5 $\mu$ s (IRS24531D)

### Package Options



### Ordering Information

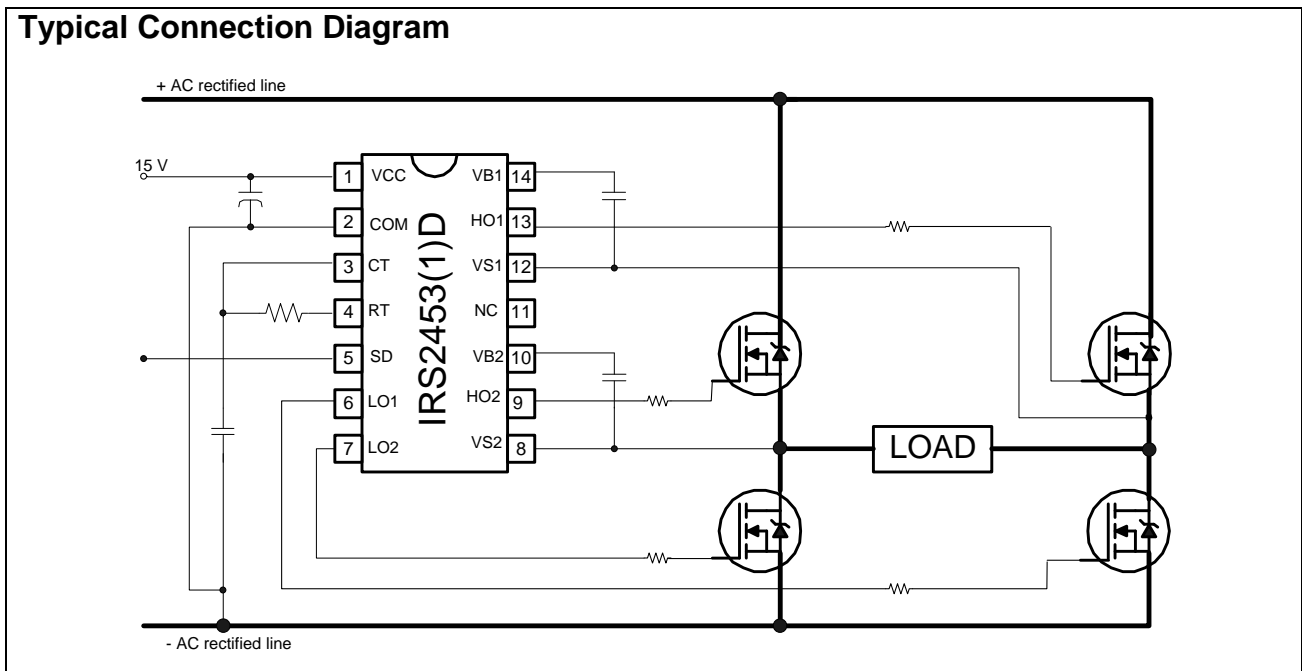
Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2453D(S)	PDIP14	Tube/Bulk	25	IRS2453DPBF
	SOIC14N	Tube/Bulk	55	IRS2453DSPBF
		Tape and Reel	2500	IRS2453DSTRPBF
IRS24531DS	SOIC14N	Tube/Bulk	55	IRS24531DSPBF
		Tape and Reel	2500	IRS24531DSTRPBF

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## Description

The IRS2453(1)D is based on the popular IR2153 self-oscillating half-bridge gate driver IC, and incorporates a high voltage full-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers, and with an under voltage lockout hysteresis greater than 1.5 V. The IRS2453(1)D also includes latched and non-latched shutdown pins.

## Typical Connection Diagram



**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Industrial <sup>††</sup>	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>		SOIC14	MSL2 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
		PDIP14	Not applicable (non-surface mount package style)
<b>ESD</b>	Machine Model	Class C (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)	
<b>IC Latch-Up Test</b>		Class I, Level A (per JESD78)	
<b>RoHS Compliant</b>		Yes	

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
VB1, VB2	High side floating supply voltage	-0.3	625	V
VS1, VS2	High side floating supply offset voltage	VB - 25	VB + 0.3	
V <sub>HO1</sub> , V <sub>HO2</sub>	High side floating output voltage	VS - 0.3	VB + 0.3	
V <sub>LO1</sub> , V <sub>LO2</sub>	Low side output voltage	-0.3	VCC + 0.3	
VRT	RT pin voltage	-0.3	VCC + 0.3	
VCT	CT pin voltage	-0.3	VCC + 0.3	
VSD	SD pin voltage	-0.3	VCC + 0.3	
IRT	RT pin current	-5	5	mA
ICC	Supply current (†)	---	25	
dV <sub>S</sub> /dt	Allowable offset voltage slew rate	-50	50	V/ns
PD	Maximum power dissipation @ T <sub>A</sub> ≤ +25 °C, PDIP14	---	1.6	W
PD	Maximum power dissipation @ T <sub>A</sub> ≤ +25 °C, SOIC14N	---	1.0	
R <sub>θJA</sub>	Thermal resistance, junction to ambient, PDIP14	---	75	°C/W
R <sub>θJA</sub>	Thermal resistance, junction to ambient, SOIC14N	---	120	
T <sub>J</sub>	Junction temperature	-55	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	---	300	

† This IC contains a zener clamp structure between the chip VCC and COM which has a nominal breakdown voltage of 15.6 V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

### Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
VBS1, VBS2	High side floating supply voltage	VCC - 0.7	VCLAMP	V
VS1, VS2	Steady state high side floating supply offset voltage	-3.0 (†)	600	
VCC	Supply voltage	V <sub>CCUV+</sub>	VCLAMP	
ICC	Supply current	(††)	5	mA
TJ	Junction temperature	-25	125	°C

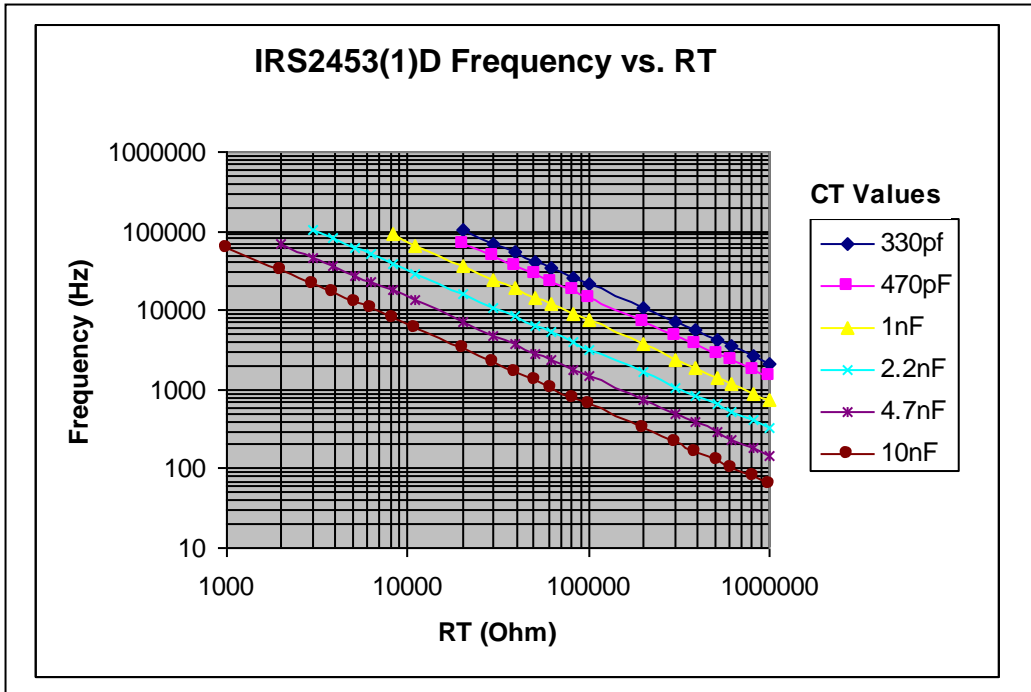
† It is recommended to avoid output switching conditions where negative-going spikes at the V<sub>S</sub> node would decrease V<sub>S</sub> below ground by more than -5V.

†† Enough current should be supplied to the VCC pin of the IC to keep the internal 15.6 V zener diode clamping the voltage at this pin.

### Recommended Component Values

Symbol	Component	Min.	Max.	Units
RT	Timing resistor value	1	---	kΩ
CT	CT pin capacitor value	330	---	pF

VBIAS (VCC, VBS) = 14 V, VS=0 V and TA = 25 °C, CLO1=CLO2 = CHO1=CHO2 = 1nF.



**Electrical Characteristics**

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 14 V,  $C_T$  = 1nF and  $T_A$  = 25 °C unless otherwise specified. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO. CLO1=CLO2=CHO1=CHO2=1nF.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Low Voltage Supply Characteristics</b>						
VCCUV+	Rising VCC under voltage lockout threshold	10.0	11.0	12.0	V	
VCCUV-	Falling VCC under voltage lockout threshold	8.0	9.0	10.0		
VCCUVH	VCC under voltage lockout hysteresis	1.5	2.0	2.4		
IQCCUV	Micropower startup VCC supply current	---	140	200	μA	$V_{CC} \leq V_{CCUV-}$
IQCC	Quiescent $V_{CC}$ supply current	---	1.3	2.0	mA	
$I_{CC\_20K}$	$V_{CC}$ supply current at $f_{osc}$ ( $R_T = 36.5 \text{ k}\Omega$ )	---	3.0	3.5		
$I_{CCFLT}$	$V_{CC}$ supply current when $SD > V_{SD}$	---	360	500	μA	
VCLAMP	VCC Zener clamp voltage	14.6	15.6	16.6	V	$I_{CC} = 5 \text{ mA}$
<b>Floating Supply Characteristics</b>						
IQBS1UV, IQBS2UV	Micropower startup VBS supply current	---	3	10	μA	$V_{CC} \leq V_{CCUV-}$ , $V_{CC} = V_{BS}$
IQBS1, IQBS2	Quiescent VBS supply current	---	30	100		
VBS1UV+, VBS2UV+	VBS supply under voltage positive going threshold	8.0	9.0	10.0	V	
VBS1UV-, VBS2UV-	VBS supply under voltage negative going threshold	7.0	8.0	9.0		
ILK1, ILK2	Offset supply leakage current	---	---	50	μA	$V_B = V_S = 600 \text{ V}$
<b>Oscillator I/O Characteristics</b>						
fOSC	Oscillator frequency	19.6	20.2	20.8	kHz	$R_T = 36.5 \text{ k}\Omega$
		88	94	100		$R_T = 7.15 \text{ k}\Omega$
d	RT pin duty cycle	48	50	52	%	$f_o < 100 \text{ kHz}$
ICT	CT pin current	---	0.05	1.0	μA	
ICTUV	UV-mode CT pin pull down current	1	5	---	mA	$V_{CC} = 7 \text{ V}$
VCT+	Upper CT ramp voltage threshold	---	9.3	---	V	
VCT-	Lower CT ramp voltage threshold	---	4.7	---		
VRT+	High level RT output voltage, $V_{CC} - V_{RT}$	---	10	50	mV	$I_{RT} = 100 \text{ }\mu\text{A}$ $R_T = 140 \text{ k}\Omega$
		---	100	300		$I_{RT} = 1 \text{ mA}$ $R_T = 14 \text{ k}\Omega$
VRT-	Low level RT output voltage	---	10	50		$I_{RT} = 100 \text{ }\mu\text{A}$ $R_T = 140 \text{ k}\Omega$
		---	100	300		$I_{RT} = 1 \text{ mA}$ $R_T = 14 \text{ k}\Omega$
VRTUV	UV-mode RT output voltage	---	0	100		$V_{CC} \leq V_{CCUV-}$

**Electrical Characteristics**

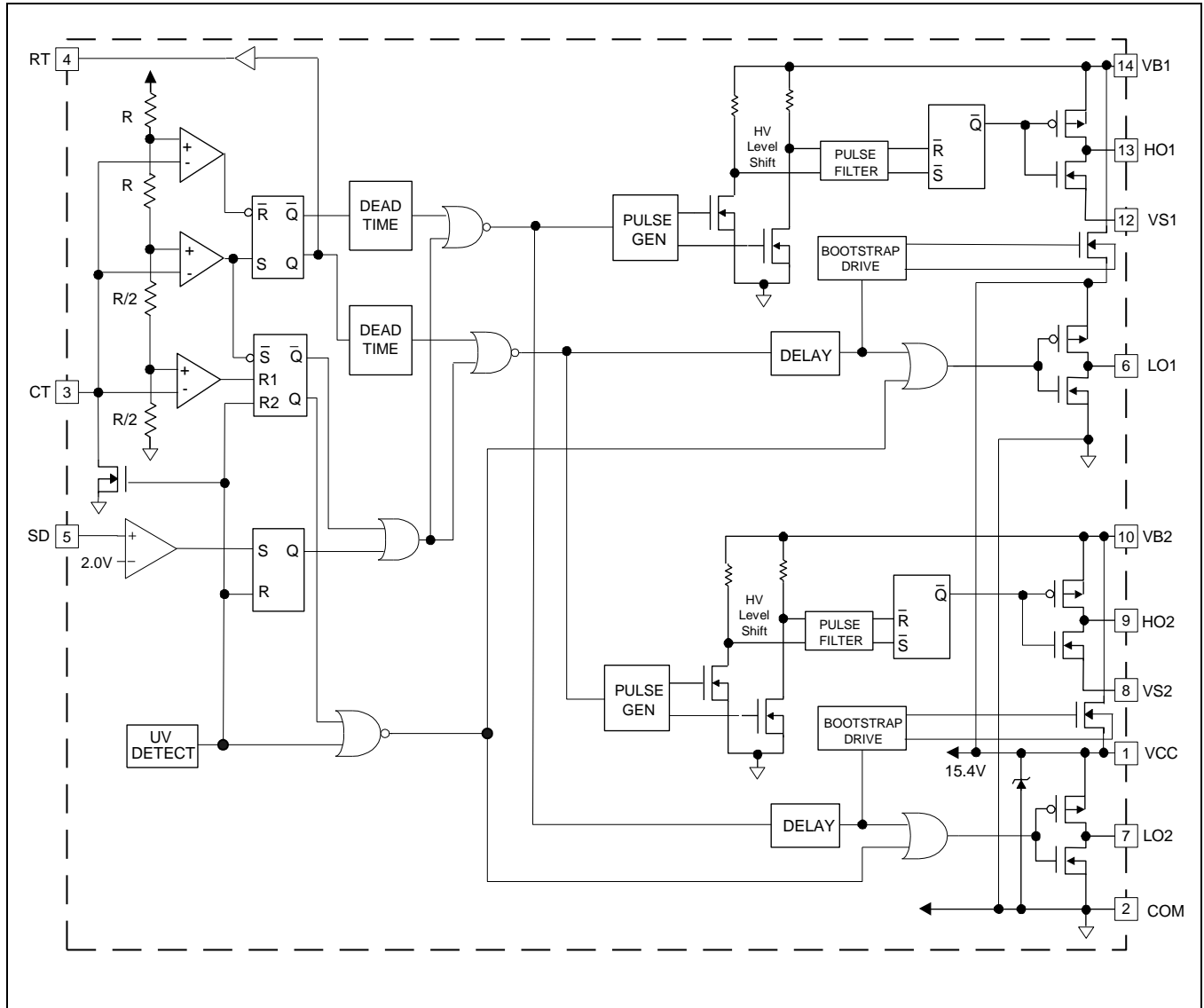
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 14 V,  $C_T$  = 1nF and  $T_A$  = 25 °C, unless otherwise specified. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads:

HO or LO. CLO1=CLO2=CHO1=CHO2=1nF.

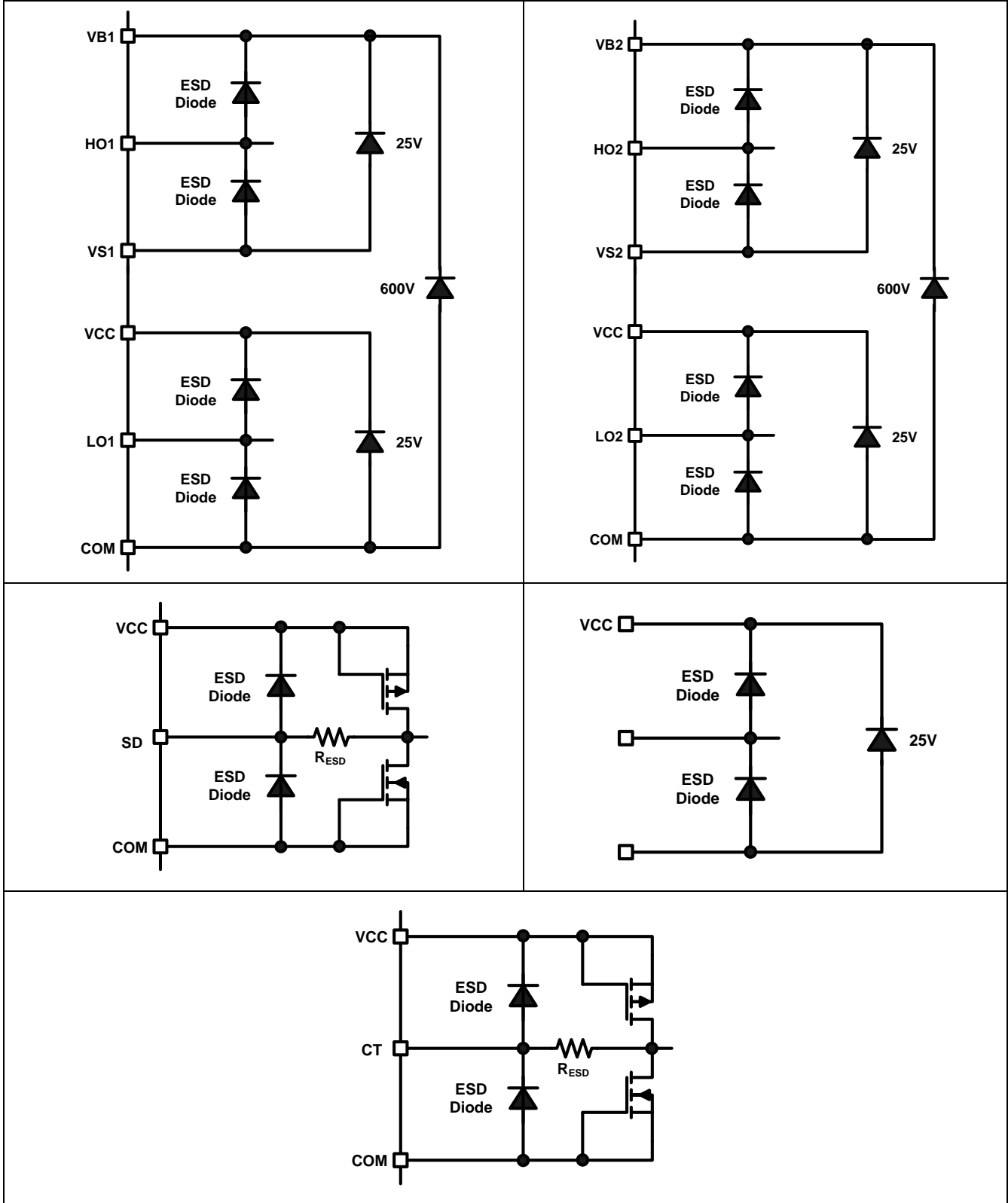
Symbol	Definition	Min	Typ	Max	Units	Test Conditions	
<b>Gate Driver Output Characteristics</b>							
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	---	$V_{CC}$	---	V	$I_O = 0$ A	
$V_{OL}$	Low level output voltage, $V_O$	---	COM	---			
$V_{OL\_UV}$	UV-mode output voltage, $V_O$	---	COM	---		$I_O = 0$ A, $V_{CC} \leq V_{CCUV-}$	
$t_r$	Output rise time	---	120	200	ns		
$t_f$	Output fall time	---	50	100			
$t_{sd}$	Shutdown propagation delay	---	250	---			
$t_d$	Output dead time (HO or LO)	IRS2453D	0.8	1.0	1.40		$\mu$ s
		IRS24531D	0.4	0.5	0.7		
$I_{O+}$	Output source current	---	180	---	mA		
$I_{O-}$	Output sink current	---	260	---			
<b>Shutdown</b>							
$V_{SD}$	Shutdown threshold at SD pin (latched)	1.8	2.0	2.3	V		
$V_{CTSD}$	CT voltage shutdown threshold (non-latched)	2.2	2.3	2.5			
$V_{RTSD}$	SD mode RT output voltage, $V_{CC} - V_{RT}$	---	10	50	mV	$I_{RT} = 100 \mu$ A, $R_T = 140$ k $\Omega$ $V_{CT} = 0$ V	
		---	100	300		$I_{RT} = 1$ mA, $R_T = 14$ k $\Omega$ $V_{CT} = 0$ V	
<b>Bootstrap FET Characteristics</b>							
$V_{B1\_ON}$ $V_{B2\_ON}$	$V_B$ when the bootstrap FET is on	13.7	14.0	---	V		
$I_{B1\_CAP}$ $I_{B2\_CAP}$	$V_B$ source current when FET is on	40	55	---	mA	$C_{BS}=0.1 \mu$ F	
$I_{B1\_10V}$ $I_{B2\_10V}$	$V_B$ source current when FET is on	10	12	---		$V_B=10$ V	



**Functional Block Diagram**



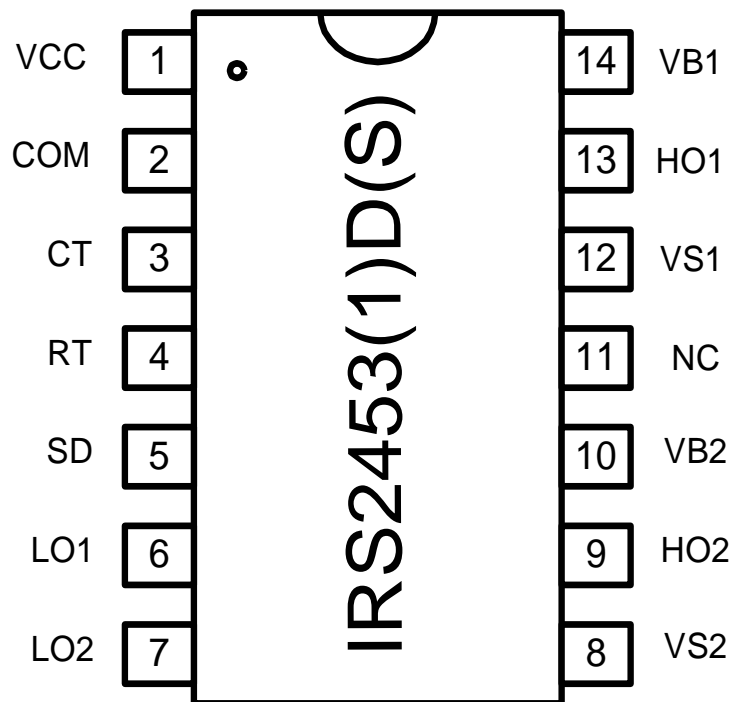
**Input / Output Pin Equivalent Circuit Diagrams:**



**Lead Definitions**

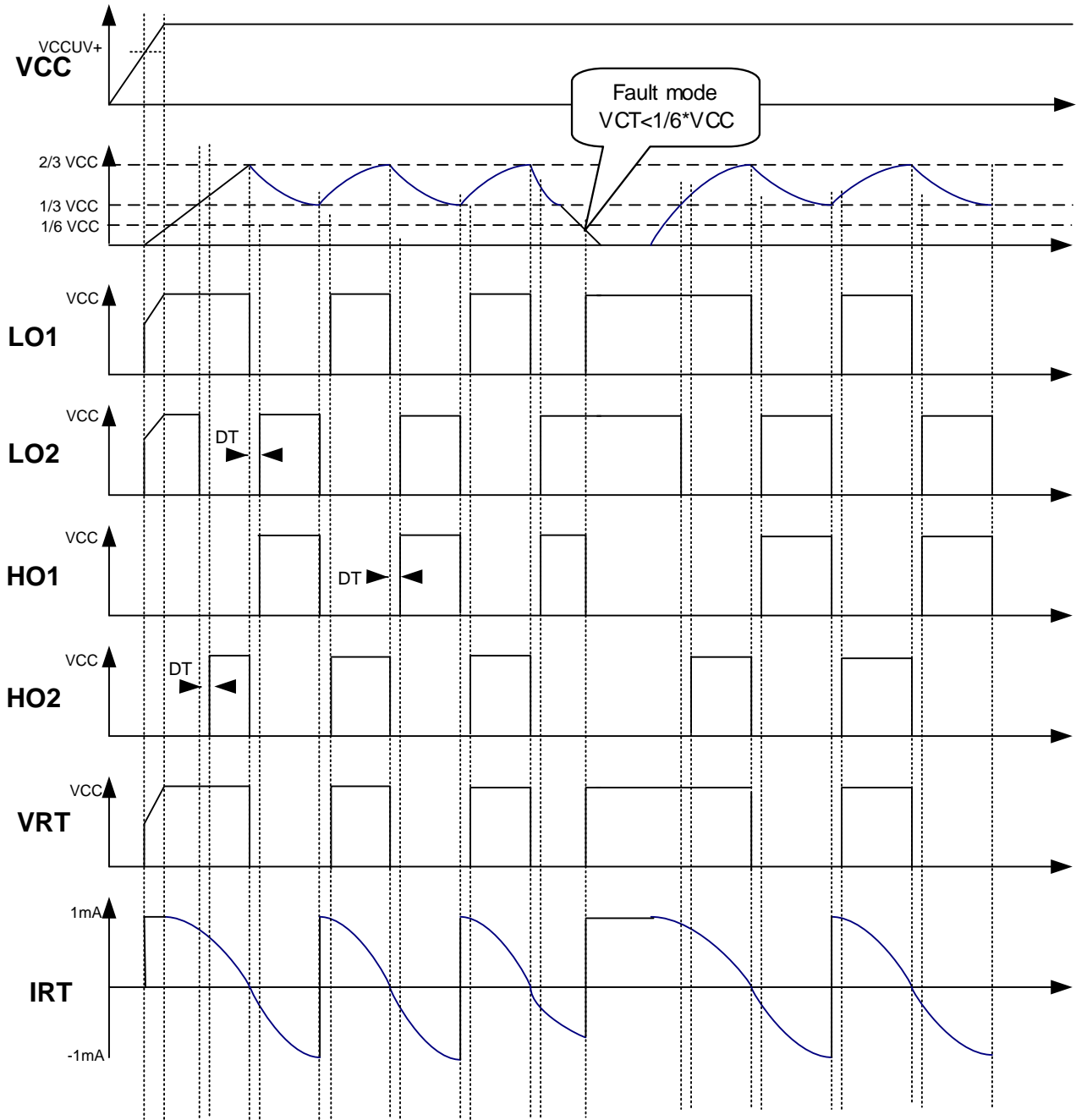
Pin	Symbol	Description
1	VCC	Logic and internal gate drive supply voltage
2	COM	IC power and signal ground
3	CT	Oscillator timing capacitor input
4	RT	Oscillator timing resistor input
5	SD	Shutdown input
6	LO1	Low side gate driver output
7	LO2	Low side gate driver output
8	VS2	High voltage floating supply return
9	HO2	High side gate driver output
10	VB2	High side gate driver floating supply
11	NC	No connect
12	VS1	High voltage floating supply return
13	HO1	High side gate driver output
14	VB1	High side gate driver floating supply

**Lead Assignment**



**Application Information and Additional Details**

**Timing Diagram**



## Functional Description

### Under-Voltage Lock-Out Mode (UVLO)

The under-voltage lockout mode (UVLO) is defined as the state the IC is in when  $V_{CC}$  is below the turn-on threshold of the IC. The IRS2453(1)D under-voltage lock-out is designed to maintain an ultra low supply current of less than 150  $\mu$ A, and to guarantee the IC is fully functional before the high and low side output drivers are activated. During under-voltage lock-out mode, the high and low side driver outputs LO1, LO2, HO1, HO2 are all low. With  $V_{CC}$  above the  $V_{CCUV+}$  threshold, the IC turns on and the output begin to oscillate.

### Normal Operating Mode

Once  $V_{CC}$  reaches the start-up threshold  $V_{CCUV+}$ , the MOSFET M1 opens, RT increases to approximately  $V_{CC}$  ( $V_{CC}-V_{RT+}$ ) and the external CT capacitor starts charging. Once the CT voltage reaches  $V_{CT-}$  (about 1/3 of  $V_{CC}$ ), established by an internal resistor ladder, LO1 and HO2 turn on with a delay equivalent to the dead time ( $t_d$ ). Once the CT voltage reaches  $V_{CT+}$  (approximately 2/3 of  $V_{CC}$ ), LO1 and HO2 go low, RT goes down to approximately ground ( $V_{RT-}$ ), the CT capacitor starts discharging and the dead time circuit is activated. At the end of the dead time, LO2 and HO1 go high. Once the CT voltage reaches  $V_{CT-}$ , LO2 and HO1 go low, RT goes to high again, the dead time is activated. At the end of the dead time, LO1 and HO2 go high and the cycle starts over again.

The frequency is best determined by the graph, Frequency vs. RT, page 3, for different values of CT. A first order approximate of the oscillator frequency can also be calculated by the following formula:

$$f \approx \frac{1}{1.453 \times RT \times CT}$$

This equation can vary slightly from actual measurements due to internal comparator over- and under-shoot delays.

### Bootstrap MOSFET

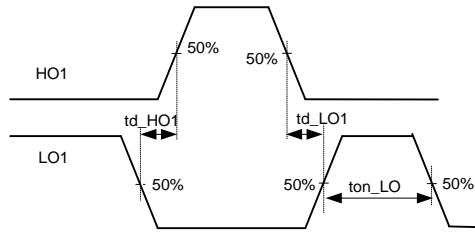
The internal bootstrap FET and supply capacitor ( $C_{BOOT}$ ) comprise the supply voltage for the high side driver circuitry. The internal bootstrap FET only turns on when the corresponding LO is high. To guarantee that the high-side supply is charged up before the first pulse on HO1 and HO2, LO1 and LO2 outputs are both high when CT ramps between zero and  $1/3 \times V_{CC}$ . LO1 and LO2 are also high when CT is grounded below  $1/6 \times V_{CC}$  to ensure that the bootstrap capacitor is charged when CT is brought back over  $1/3 \times V_{CC}$ .

### Non-Latched Shutdown

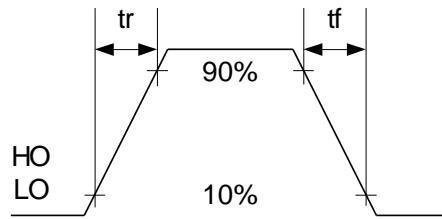
If CT is pulled down below  $V_{CTSD}$  (approximately 1/6 of  $V_{CC}$ ) by an external circuit, CT is not able to charge up and oscillation stops. HO1 and HO2 outputs are held low. LO1 and LO2 outputs remain high while VCT remains below  $V_{CT-}$ . enabling the bootstrap capacitors to charge. This state remains until the CT input is released and oscillation can resume.

### Latched Shutdown

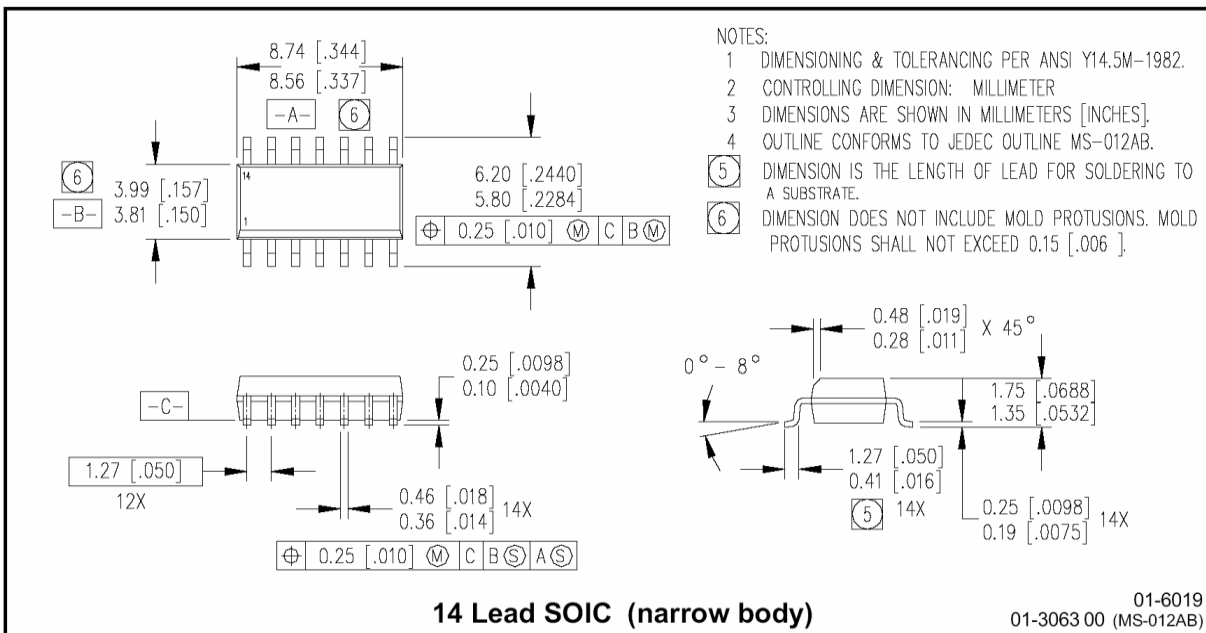
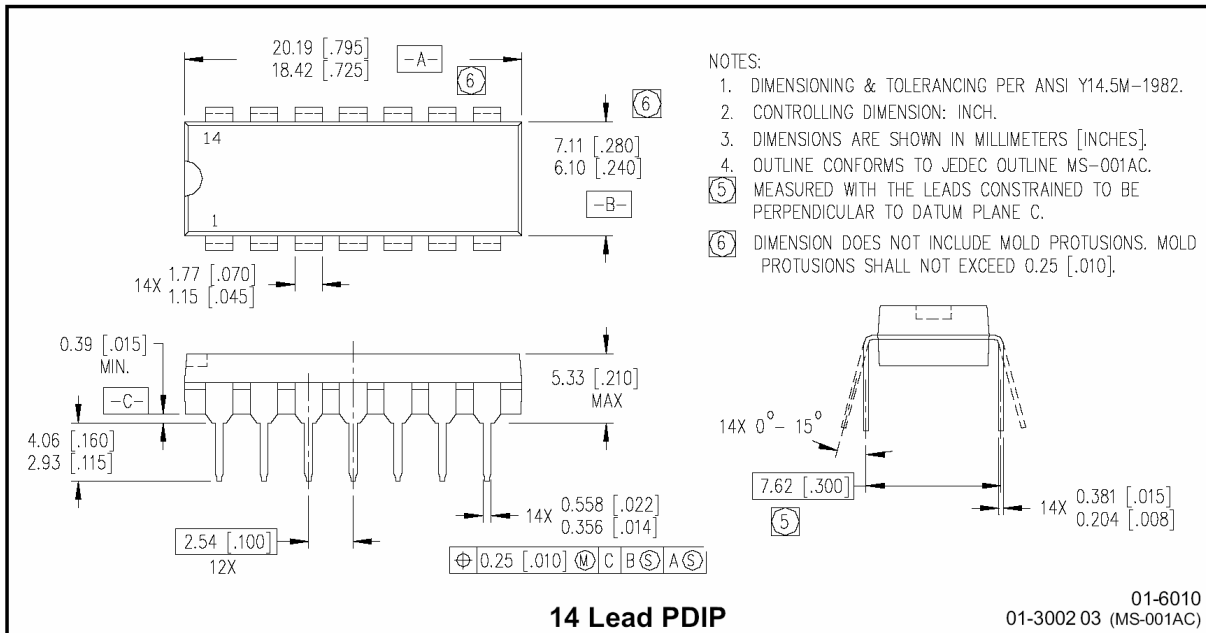
When the SD pin is brought above 2 V, the IC goes into fault mode and all outputs are low.  $V_{CC}$  has to be recycled below  $V_{CCUV-}$  to restart. The SD pin can be used for over-current or over-voltage protection using appropriate external circuitry.



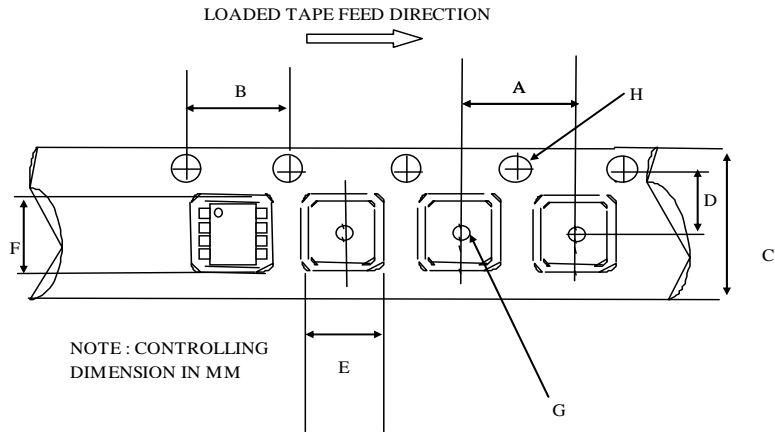
**Deadtime Waveform**



**Rise and Fall Time Waveform**

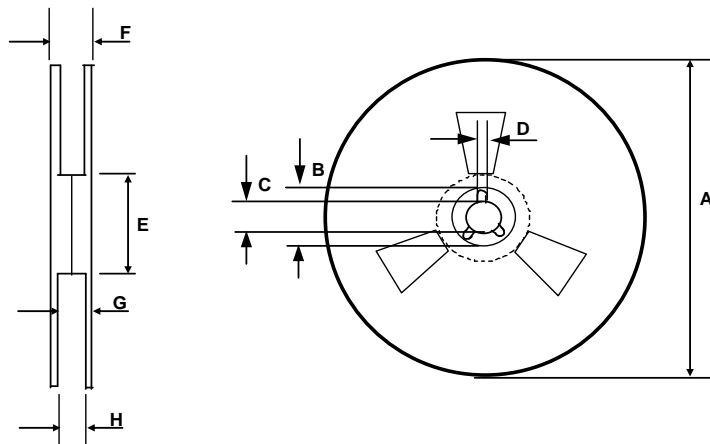
**Package Details**


**Tape and Reel Details**



**CARRIER TAPE DIMENSION FOR 14SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

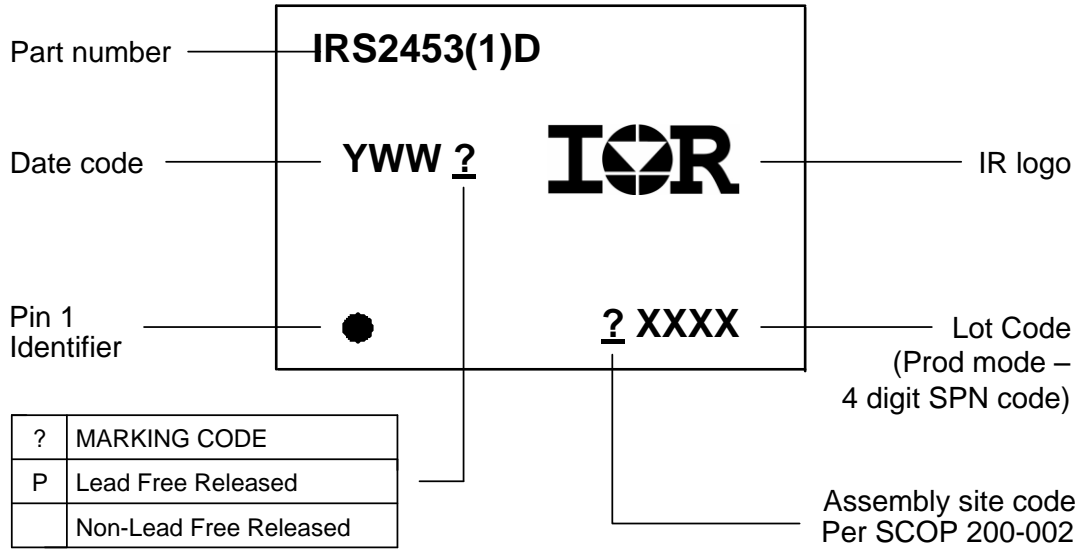


**REEL DIMENSIONS FOR 14SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724



**Part Marking Information**



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